

AD-A177 006

A SINGLE CHIP LSI HIGH-SPEED FUNCTIONAL TESTER(U)  
STANFORD UNIV CA COMPUTER SYSTEMS LAB  
J MIYAMOTO ET AL. 16 SEP 86 MDA903-83-C-0335

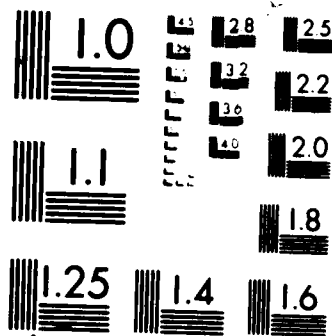
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XEROCOPY RESOLUTION TEST CHART

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## A Single Chip LSI High-Speed Functional Tester

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September 16, 1986

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### Abstract

A new architecture of single chip tester, DGR, will be proposed. It generates test vectors designated by the internal memory data, and simultaneously, detects the DUT data, being overwritten on that memory. A prototype chip designed by 3um CMOS contains 64.5K transistors in a die size of 9.2mm by 7.9mm, and dissipates less than 300mW at an operating frequency of 10MHz.

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\*On leave during 1985-86 from Toshiba Corporation.

### Summary

Recently, we have seen an explosion in the development of application specific ICs, (ASICs) for use in systems ranging from computers to communications. However, testing these chips after they are manufactured remains a serious problem, especially for high speed tests. In this paper, we will propose a one-chip function tester, DGR (Data Generator and Receiver), as one solution for this problem.

As shown in Fig. 1, the DGR is composed of three main parts: memory, address control, and DUT(Device Under Test) pin control. The memory stores the test vectors for the DUT. Each vector contains 2bits per DUT pin. One bit is "state" data, which determines whether the pin is a driver or receiver, and the other is "value" data, which determines the output level if the pin is a driver, or the expected value if it is a receiver. The value data is overwritten by the detected value, during the measurement. The address control block sets the sequence of memory locations during a test, and consists of counter, comparator, and a set of special registers. The registers include a start, stop and branch addresses, and registers that store the addresses where errors occur. The DUT control block has a 16bit register for each DUT pin, which configures the pin for testing. Each pins can be programmed for RZ (return to zero) NRZ codes, have its output transitions synchronized to either clock, sample its input on either clock, be active high or active low, etc. In addition each pin is short circuit protected (and indicates this condition with a flag), compares the incoming data with the expected data and indicates errors, and can compare data for conditional branches.

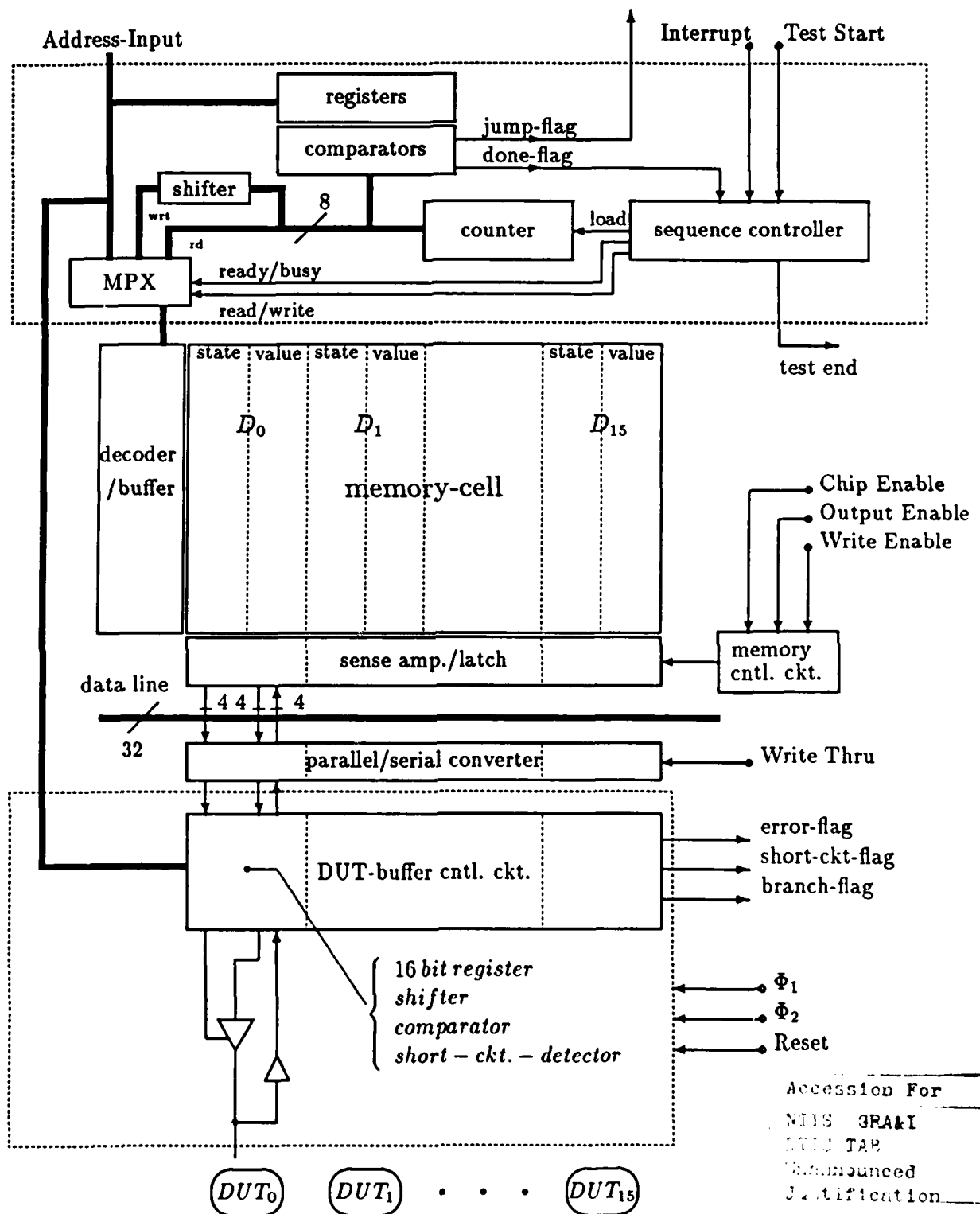
Obtaining a high speed vector rate from the DGR was our key performance goal. To increase the vector rate, the state and value data is read 4bits at a time from the memory and is sequentially sent to the DUT control block as shown in Fig. 2. The pipelining of the memory fetch allows the vector rate to be twice the memory cycle time. Nevertheless, we felt the address access time would still limit the overall performance. To reduce this delay, we used a high speed memory organization, taking advantage of the synchronous operation of the memory during vector reads, as is depicted in Fig. 3. The memory can be operated in an asynchronous mode, and looks like a conventional static RAM through the host interface.

The design of the DGR allows the tester to be made both wider and deeper by simply using more DGR chips. As shown in Fig. 4, adding chips in parallel increases the number of DUT pins, while cascading chips increases the vector depth. To cascade two DGRs, the Test End signal directly becomes the Test Start signal of the next DGR; all the flag output are open drain buffers allowing them to be wired ORed together. In addition, DGR supports a lower speed read/write through mode for unlimited test vectors, as explained in Fig. 5. In this mode, the state and value data are directly provided on vector at a time through the host interface, synchronized to the DGR through the "Data Request" pin.

A prototype DGR was designed in a 3 $\mu$ , double Al CMOS technology, contains 64.5K transistors in a die size of 9.2mm by 7.9mm, and dissipates less than 300mW at an operating frequency of 10MHz. A die photo of the device is shown in Fig. 6. One DGR supports 192 test vectors for 16 DUT pins, and fits into 84 pin package. The technology limited the size of the on chip RAM to 6Kbits, limiting the vector depth of each chip. With a more advanced CMOS technology it would be easy to greatly increase the vector depth.

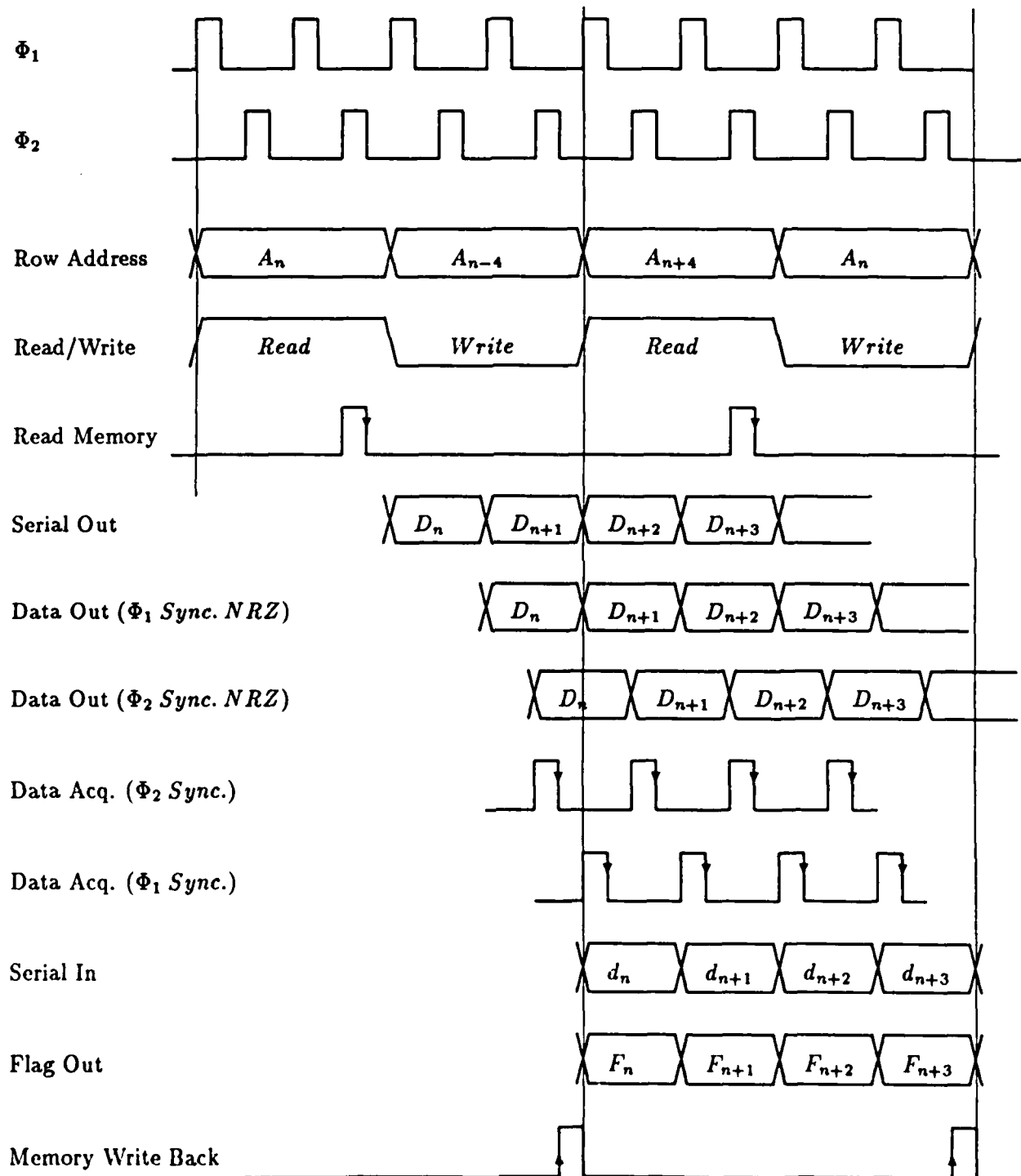
### Acknowledgements

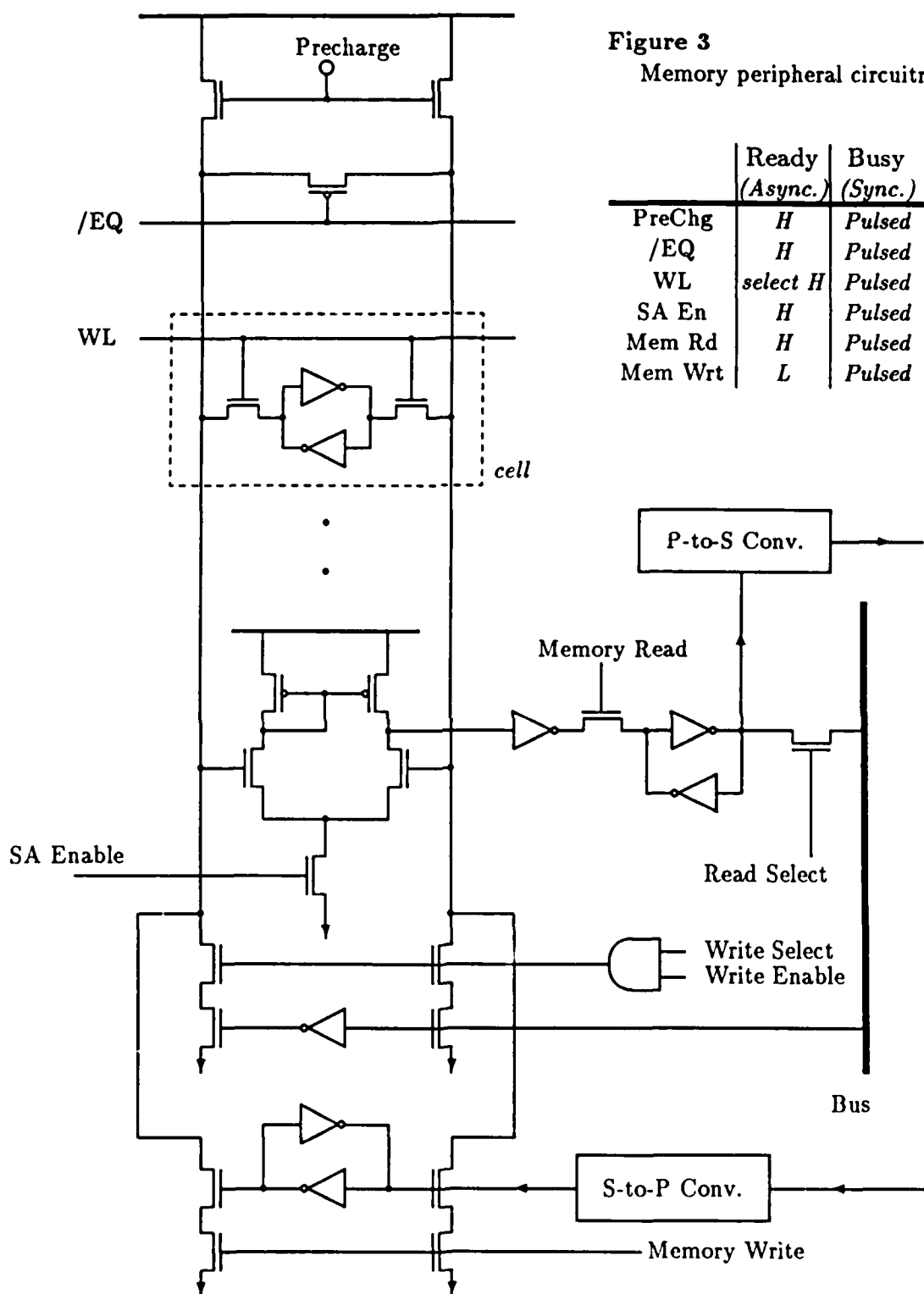
The development of the DGR was partially supported by the Defense Advanced Project Research Agency under Contract No. MDA903-83-C-0335. Mr. Miyamoto was supported by the Toshiba Corporation. Fabrication support through MOSIS is also gratefully acknowledged.



**Figure 1** The block diagram of DGR

Figure 2 Typical measurement sequences





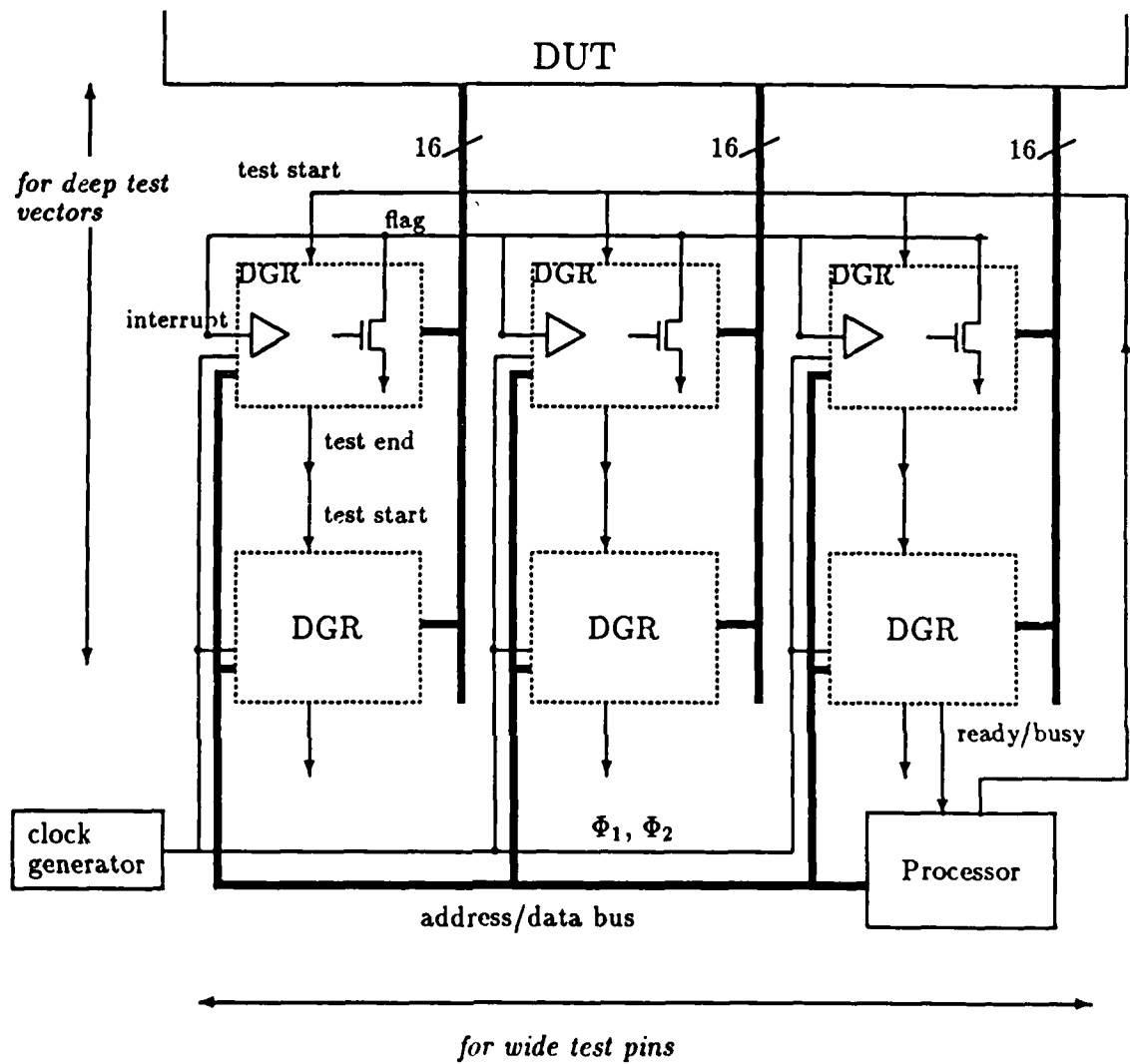


Figure 4 Parallel and cascade connections of DGR

Figure 5 Read/Write through mode of DGR

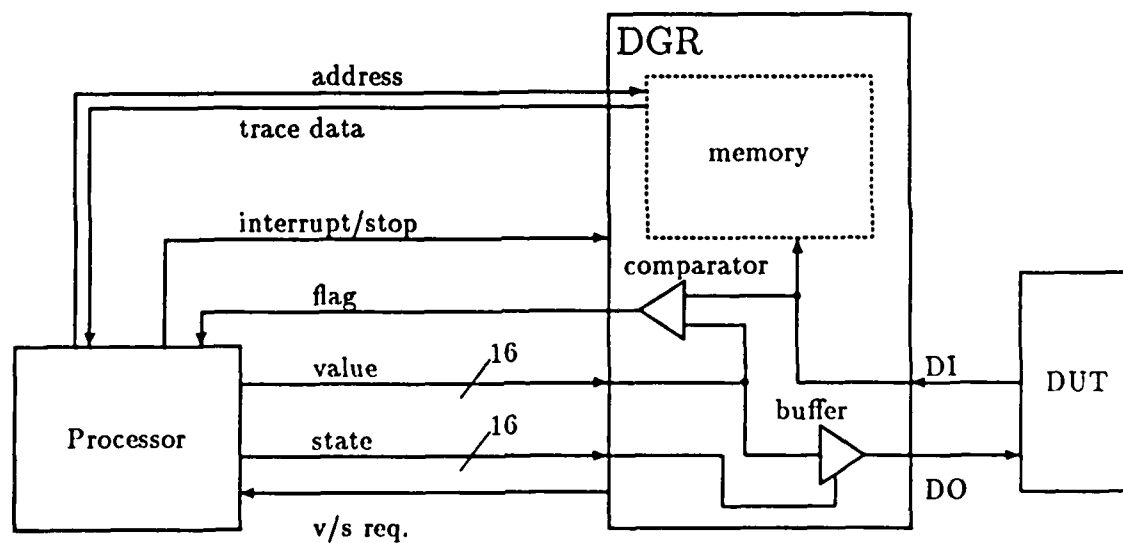
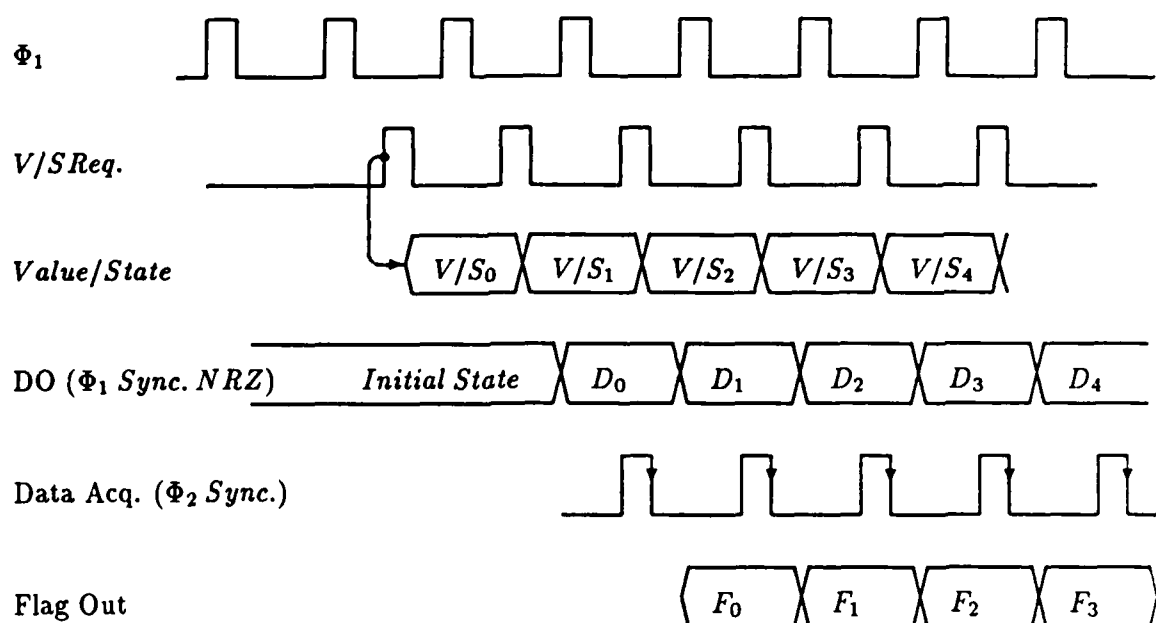
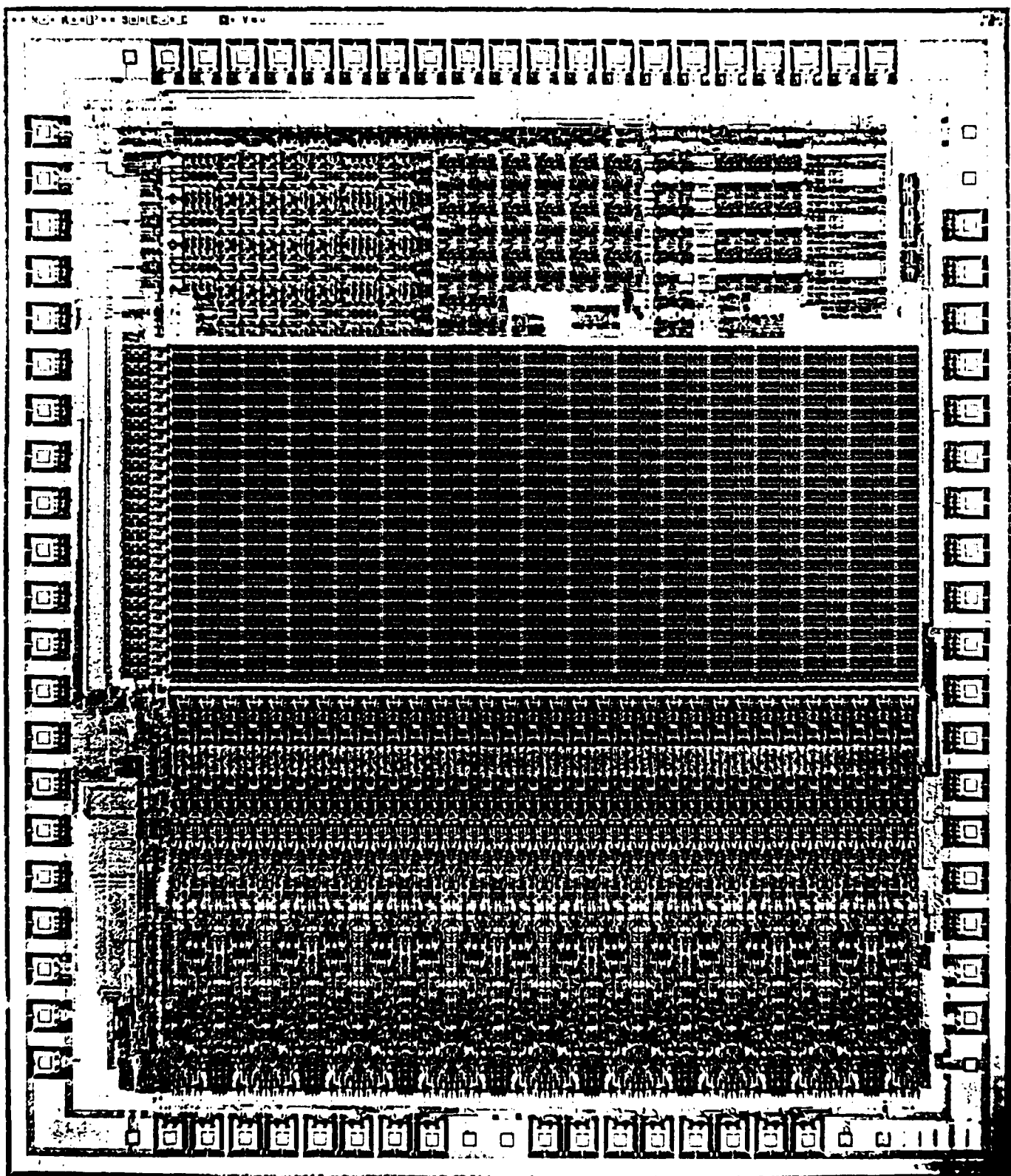


Figure 6 The die photo of DGR



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